IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent Application

Inventor(s)	Charles D. Carr Lu Fang Dhiraj H. Malkani
Case	3-10-3
Conf. No.	2372
Serial No.	09/872,306
Group Art Unit	2874
Filing Date	June 1, 2001
Examiner	Joshua L. Pritchett
Title	**MEMS Device**

COMMISSIONER FOR PATENTS
ALEXANDRIA, VA 22313

SIR:

BRIEF ON APPEAL

I. INTRODUCTION

Appellants submit the foregoing brief pursuant to a Notice of Appeal mailed December 24, 2003, from a decision of the Examiner dated December 15, 2003, finally rejected claims 1-17 of the above-identified application.

II. REAL PARTY IN INTEREST

Agere Systems, Inc. is the real party in interest by virtue of an Assignment recorded in the United States Patent and Trademark Office on January 4, 2002.

III. RELATED APPEALS AND INTERFERENCES

This is the first appeal in the above-identified application.

IV. STATUS OF CLAIMS

The present application contains claims 1-17, where all claims are under a "Final" rejection. The attached Appendix A contains a complete copy of the claims now pending in the application.

Appellants appeal the Final Rejection by the Examiner of all claims 1-10.

V. STATUS OF AMENDMENTS

In the Advisory Action dated December 15, 2003, the Examiner stated that the proposed Amendment of November 20, 2003 would not be entered in that is "is not deemed to place the application in better form for appeal by materially reducing or simplifying the issues for appeal".

VI. SUMMARY OF THE INVENTION

Appellants' invention relates to the field of Micro Electromechanical System (MEMS) devices and, as discussed in the specification beginning at page 2, line 5, relates to "a device comprising an array of electrostatically activated members (e.g., mirrors) formed in a layer comprising silicon, and a substrate comprising a ceramic material and including conductors formed on a major surface of the substrate and in via holes formed in the substrate, the conductors being positioned so as to selectively operate the array of members". Finally rejected independent claim 1 defines a "device" as including "a substrate comprising a ceramic material and including conductors formed on a major surface thereof and in via holes formed therethrough the conductors being positioned with respect to and separate from the silicon layer so as to *selectively operate the array of members using an electrostatic force* such that the utilization of conductors on the silicon layer is not required" [emphasis added]. Independent method claim 13 includes the step of "forming an array of *electrostatically activated* members in a layer of silicon" [emphasis added}.

VII. ISSUES

The issues on appeal are: (1) whether the subject matter of claims 1, 2, 4, 5, 11, 13, 14 and 17 is rendered obvious by the combination of US Patent 6,433,411 (Degani),

US Patent 5,952,712 (Ikuina) and Japanese Patent 09261975 (Higuchi); (2) whether the subject matter of claim 4 is rendered obvious by the combination of Degani, Ikuina and Higuchi (as above), in further view of a reference by Lin; (3) whether the subject matter of claim 5 is rendered obvious by the combination of Degani, Ikuina and Higuchi (as above), in further view of US Patent 6,393,187 (Engelberth); (4) whether the subject matter of claims 7 and 9 is rendered obvious by the combination of Degani, Ikuina and Higuchi (as above), in further view of an article by Imanaka; (5) whether the subject matter of claim 8 is rendered obvious by the combination of Degani, Ikuina and Higuchi (as above), in further view of Lin (as above); (6) whether the subject matter of claim 10 is rendered obvious by the combination of Degani, Ikuina and Higuchi (as above), in further view of US Patent 6,329,607 (Fjelstad) and US Patent 6,284,656 (Farrar); (7) whether the subject matter of claim 12 is rendered obvious by the combination of Degani, Ikuina and Higuchi, Lin and Imanaka; and (8) whether the subject matter of claims 15 and 16 is rendered obvious by the combination of Degani, Ikuina and Higuchi, in further view of US Patent 5,995,688 (Aksyuk).

Appellants request that the Board of Patent Appeals and Interferences reverse the decision of the Examiner finally rejecting these claims and find all claims 1-17 to be in condition for allowance over the cited references.

VIII. GROUPING OF CLAIMS

For the purposes of this appeal, claims 1-11 stand or fall together, claim 12 stands or falls alone, and claims 13-17 stand or fall together.

IX. ARGUMENTS

A. 35 USC § 103(a) Rejection - Claims 1, 2, 4, 6, 11, 13, 14 and 17

In the Office action dated September 25, 2003, the Examiner issued a Final Rejection of the above-cited group of references under 35 USC 103(a) as being unpatentable over Degani, Ikuina, and Higuchi. In particular, the Examiner stated that "Degani further lacks conductors formed on a major surface of the substrate. Ikuina teaches the use of conductors (17) on a ceramic substrate (12) with via holes (15) in the substrate and the substrate connected to a silicon layer (11). *It is not clear if the*

conductors (17) of Ikuina are inside via holes (15) therefore the examiner will assume the conductors are not passing through the via holes" [emphasis added].

In response, appellants assert that Ikuina does indeed clearly describe the utilization of "conductors 17" that pass through via holes 15. The Examiner is referred to FIG. 1 of Ikuina that illustrates "conductor 17" as the layer marked with the metallic PTO designation ("///////"), and obviously connecting conductor 14 to conductor 16 through via hole 15. The Examiner is also referred to Ikuina at column 4, beginning at line 36, which states: "The electrode 14 formed on the integrated circuit of the LSI chip 11 is connected to the electrode 16, formed on the package 12 to be connected to the board, with the connecting conductor 17 through the through hole 15" [emphasis added]. Thus, in the arrangement of Ikuina, a direct, physical electrical connection is made between a first electrode on a ceramic substrate and a second electrode on a silicon substrate.

Therefore, appellants conclude that Ikuina *teaches away* from the use of an "electrostatic force" such that "the utilization of conductors on the silicon layer is not required", as defined in presented claim 1 (see Appendix), or conductors that "remain separated from" the silicon layer so as to "operate the array of mirrors using an electrostatic force" as defined in independent claim 12 (see Appendix). The remaining independent claims contain similar language.

On this basis, appellants assert that the combination of Degani, Ikuina and Higuchi cannot be found to render obvious the subject matter of the finally-rejected claims and therefore respectfully request the Board of Appeals to reconsider these arguments, reverse the Examiner's rejection, and find claims 1, 2, 4, 6, 11, 13, 14 and 17 to be in condition for allowance.

B. 35 USC § 103(a) Rejection - Claim 3

The Examiner issued a separate Final rejection of claim 3 under 35 USC 103(a) as being unpatentable over Degani in view of Ikuina and Higuchi (as applied above), in further view of an article by Lin (of record), where Lin was cited as teaching that an array of size 3x3 can easily be expanded to an array of 8x10.

Regardless of the teaching of Lin, appellants assert that the combination of cited references still lacks any teaching of controlling the operation of an array of

electrostatically activated members without including an electrical contact on the silicon layer of the device structure. For the reasons discussed above, the cited Ikuina reference does indeed disclose and teach the use of a "conductor" 17 through a via hole 15 between a first conductor 14 and a second conductor 16.

Appellants therefore respectfully request the Board of Appeals to review this rejection and reveries the Examiner's finding, and allow claim 3 to also pass to issue.

C. 35 USC § 103(a) Rejection - Claim 5

Claim 5 was next rejected by the Examiner under 35 USC 103(a) as being unpatentable over Degani, Ikuina and Higuchi (as above, applied to claim 1), in further view of Engleberth, where Engleberth was cited by the Examiner as teaching the use of a metal layer deposited on a silicon layer. However, the Engleberth reference is not germane to the subject matter of MEMS technology, but to an optical fiber-based free space optical switch. Regardless of the subject matter of Engleberth, however, it is asserted that the combination of Engleberth with Degani, Ikuina and Higuchi still lacks any teaching of using a separate silicon layer and ceramic substrate, as defined by claim 5 (based on independent claim 1).

Appellants therefore respectfully request the Board of Appeals to review the Examiner's final rejection of claim 5 and find this claim to instead be in condition for allowance.

D. 35 USC § 103(a) Rejection - Claims 7 and 9

Claims 7 and 9 were issued a Final rejection by the Examiner under 35 USC 103(a) as being unpatentable over Degani in view of Ikuina and Higuchi (as applied to claim 1), in further view Imanaka, where Imanaka was cited for its teaching of the properties of a ceramic material (in particular, for the use of aluminum nitride and issues regarding its roughness). However, the combination of Imanaka with Degani, Ikuina and Higuchi still lacks any teaching of using separate silicon and ceramic members for the optic and electronic portions of a MEMS device, as defined by independent claim 1, from which both claims 7 and 9 depend.

Appellants therefore respectfully request the Board of Appeals to review this Final rejection of the Examiner and find claims 7 and 9 in condition for allowance.

E. 35 USC § 103(a) Rejection - Claim 8

The Examiner next issued a Final rejection of claim 8 under 35 USC 103(a) as being unpatentable over Degani in view of Ikuina and Higuchi (as applied to claim 1), in further view of Lin (as above). The Examiner particularly cited Lin as teaching the use of a substrate with a flatness less than 10 microns (particularly, Lin teaches a flatness of 0.5 microns). Regardless of the teaching of Lin, appellants assert that the cited combination still lacks any teaching regarding the use of a first element (a silicon layer) to form the actual MEMS array and a second element (a ceramic substrate) to form the electronics for controlling the MEMS array. Without this teaching, appellants assert that the cited combination cannot be found to render obvious the teachings of claim 8, which ultimately depends from claim 1 (as discussed above).

Appellants therefore respectfully request the Board of Appeals to review the Examiner's final rejection and, instead, find claim 8 to be in condition for allowance.

F. 35 USC § 103(a) Rejection - Claim 10

Claim 10 was issued a Final rejection by the Examiner under 35 USC 103(a) as being unpatentable over Degani in view of Ikuina and Higuchi (as applied to claim 1), in further view of Fjelstad and Farrar. The Fjelstad and Farrar references were cited by the Examiner as teaching particular line width and spacing requirements for conductors in microelectronic structures. However, this combination still lacks any teaching of utilizing separate substrates for MEMS devices and their associated conductors, as defined by independent claim 1, from which claim 10 depends.

Appellants thus respectfully request the Board of Appeals to reconsider the Examiner's final rejection and find claim 10 to be in condition for allowance.

G. 35 USC § 103(a) Rejection - Claim 12

Independent claim 12 was finally rejected by the Examiner under 35 USC 103(a) as being unpatentable over Degani, in view of Ikuina, Higuchi, Lin and Imanaka, for all of the reasons discussed above in association with the rejection of the previous claims. In light of the lack of teaching in Ikuina regarding the use of a separate ceramic substrate to provide and support *all* of the "conductors" that are "positioned so as to selectively operate the array of mirrors" as defined by claim 12, appellants assert that this combination of references cannot be found to render obvious the subject matter of claim 12. It is therefore respectfully requested that the Board of Appeals review the Examiner's final rejection and instead find claim 12 to be allowable over the cited combination.

H. 35 USC § 103(a) Rejection - Claims 15 and 16

The Examiner further issued a Final rejection of claims 15 and 16 under 35 USC 103(a) as being unpatentable over Degani in view of Ikuina and Higuchi (as applied to claim 13, above), in further view of Aksyuk, where the Aksyuk reference was cited by the Examiner as teaching bonding of a MEMS substrate to an SiOB substrate. However, there is no teaching in Aksyuk of bonding a silicon layer (supporting MEMS devices) to a *ceramic* substrate supporting MEMS electronics. Appellants thus assert that the combination of Aksyuk with Degani, Ikuina and Higuchi cannot be found to render obvious the subject matter of the present invention as defined by claims 15 and 16.

Appellants therefore respectfully request the Board of Appeals to review this rejection, reverse the Examiner's finding, and allow claims 15 and 16 to pass to issue.

X. CONCLUSION

For all of the reasons expressed above, the Examiner's various rejections under 35 USC § 103(a) are considered to lack merit and thus mandate reversal. Appellants solicit such action from the Board of Appeals at this time.

Respectfully submitted,

Charles D. Carr
Lu Fang
Dhiraj H. Maklani

By: Wendy W. Koba
Wendy W. Koba
Reg. No. 30509
Attorney for applicant
610-346-7112

Date: 2/24/04

Appendix A -- Pending Claims for Appln. No. 09/872,306

1. A device comprising:

an array of electrostatically activated members formed in a layer comprising silicon; and

a substrate comprising a ceramic material and including conductors formed on a major surface thereof and in via holes formed therethrough the conductors being positioned with respect to and separate from the silicon layer so as to selectively operate the array of members using an electrostatic force such that the utilization of conductors on the silicon layer is not required.

2. The device according to claim 1 wherein the members are rotatable mirrors.

3. The device according to claim 1 wherein the array comprises a structure of at least eight members by at least ten members.

4. The device according to claim 1 wherein the array is separated from the ceramic substrate by a spacer layer.

5. The device according to claim 1 further comprising a layer of metal on a major surface of the silicon layer.

6. The device according to claim 2 wherein the mirrors are adapted to rotate about at least two axes.

7. The device according to claim 1 wherein the ceramic substrate comprises aluminum nitride (AlN).

8. The device according to claim 1 wherein the substrate has a flatness of less than or equal to 10 microns.

9. The device according to claim 1 wherein the substrate has a surface roughness of less than or equal to 1 micron.

10. The device according to claim 1 wherein the conductors have a line width of less than 2 microns and a spacing less than 2 microns.

11. The device according to claim 1 wherein the conductors positioned to operate one member from the array of electrostatically activated members comprise an array of at least four conductors extending through separate via holes.

12. A device comprising:

an array of at least 8x10 mirrors rotatable about at least two axes formed in a layer comprising silicon;

a spacer layer formed over a surface of the silicon layer; and

a substrate comprising a ceramic material having a flatness of less than or equal to 10 microns and a surface roughness of less than or equal to 1 micron, said substrate including conductors formed on a major surface thereof and in via holes formed therethrough, the conductors being positioned with respect to the silicon layer so as to selectively operate the array of mirrors using an electrostatic force, wherein the conductors remain separated from said silicon layer and are positioned to operate a mirror comprise an array of at least four conductors extending through separate via holes.

13. A method of forming a device comprising:

forming an array of electrostatically activated members in a layer of silicon; and

mounting said silicon layer over a substrate comprising a ceramic material which includes conductors formed on a major surface of the substrate and in via holes formed in the substrate, the silicon layer being mounted so as to position the members with respect to the conductors to permit selective operation of the members.

14. The method according to claim 13 wherein the members are movable mirrors.

15. The method according to claim 13 wherein the silicon layer is mounted using an epoxy bond.

16. The method according to claim 13 wherein the silicon layer is mounted using a solder bond.

17. The method according to claim 13 wherein a spacer layer is included between the silicon layer and the ceramic substrate.